What is claimed is:

1. A method comprising:

receiving a first program unit in a parallel computing environment, the first program unit including a reduction operation associated with a set of variables;

translating the first program unit into a second program unit, the second program unit to associate the reduction operation with a set of one or more instructions operative to partition the reduction operation between a plurality of threads including at least two threads; and

translating the first program unit into a third program unit, the third program unit to associate the reduction operation with a set of one or more instructions operative to perform an algebraic operation on the variables.

2. The method of claim 1 further comprising encapsulating the reduction operation with the instructions associated with the third program unit.

3. The method of claim 1 further comprising reducing the variables logarithmically.

4. The method of claim 1 further comprising translating the first program unit into the second program unit utilizing, in part, a source-code to source-code translator.

5. The method of claim 1 further comprising translating the first program unit into the third program unit utilizing, in part, a source-code to source-code translator.

6. The method of claim 1 further comprising associating the plurality of threads each with a unique portion of the set of variables.

7. The method of claim 6 further comprising combining, in part, the variables associated with the plurality of threads in a pair-wise reduction operation.

8. An apparatus comprising:

a memory including a shared memory location;

a translation unit coupled with the memory, the translation unit to translate a first program unit including a reduction operation associated with a set of at least two variables into a second program unit, the second program unit to associate the reduction operation with one or more instructions operative to partition the reduction operation between a plurality of threads including at least two threads;

a compiler unit coupled with the translation unit and the shared-memory, the compiler unit to compile the second program unit; and

a linker unit coupled with the compiler unit and the shared-memory, the linker unit to link the compiled second program with a library.

9. The apparatus of claim 8 wherein the second program unit associates a set of one or more instructions with the reduction operative to encapsulate the reduction operation.

10. The apparatus of claim 8 wherein the variables in the set of variables are each uniquely associated with the plurality of threads and the library includes instructions operative to combine, in part, the variables associated with the plurality of threads.

11. The apparatus of claim 10 wherein the library includes instructions operative to combine, in part, the variables in a pair-wise reduction.

12. The apparatus of claim 8 further comprising a set of one or more processors to host the plurality of threads, the plurality of threads to execute instructions associated with the second program unit.

13. The apparatus of claim 8 wherein the second program includes a callback routine and the callback routine is associated with instructions operative to

perform an algebraic operation on at least two variables in the set of variables.

14. The apparatus of claim 13 wherein the library is operative to call the callback routine to perform, in part, a reduction on at least two variables in the set of variables.

15. A machine-readable medium that provides instructions, that when executed by a set of one or more processors, enable the set of processors to perform operations comprising:

receiving a first program unit in a parallel computing environment, the first program unit including a reduction operation associated with a set of variables;

translating the first program unit into a second program unit, the second program unit to associate the reduction operation with a set of one or more instructions operative to partition the reduction operation between a plurality of threads including at least two threads; and

translating the first program unit into a third program unit, the third program unit to associate the reduction operation with a set of one or more instructions operative to perform an algebraic operation on the variables.

16. The machine-readable medium of claim 15 further comprising encapsulating the reduction operation with a set of one or more instructions.

17. The machine-readable medium of claim 15 further comprising translating the first program unit into the second program unit utilizing, in part, a source-code to source-code translator.

18. The machine-readable medium of claim 15 further comprising reducing the variables, in part, logarithmically.

19. The machine-readable medium of claim 15 further comprising translating the first program unit into the third program unit utilizing, in part, a source-code to source-code translator.

20. The machine-readable medium of claim 15 further comprising the second program unit utilizing, in part, the third program unit to perform a reduction operation on the set of variables.